Efficient Design of Carry Look Ahead Adder Consuming CMOS Low Power Logic Strategies with Power Calculation Estimation

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In digital circuits, the speed is significantly enhanced due to reduced capacitance at each evaluation node of dynamic circuits. The power reduction can be achieved due to reduced adder cell size with minimal race problem. Clocked CMOS logic has been implemented to design low power indulgence CMOS logic. The main motive of such logics is to create clocked structures that incorporate latches or interface with other dynamic states of logic. The gates have similar input capacitance as complementary gates but high rise and fall times due to the series clocked transistors. This alteration to the clock in the CMOS logic leads to a single clock pre-charge and evaluation of a group of dynamic blocks. In this paper Carry look ahead is implemented with low power logics and not only proven that it is preferred for long adders, the dynamic power utilization is also radically reduced by 10% on silicon.

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Introduction

Complementary metal oxide semiconductor (CMOS) is a widely used technology for designing integrated circuits. By using CMOS technology microcontrollers, microprocessors, and other digital logic circuits are implemented. CMOS technology is implemented in designing many analog circuits such as highly integrated transceivers for communication, image sensors data converters, and for many other types. Main assets of CMOS technology devices are high immunity to noise and low static power consumption.

In this technology one transistor in the pair is always in off state, and the significant power consumption by the series combination is done only during switching between on and off states. As a result CMOS devices will not generate as much ravage heat as other styles of logic. In CMOS the density of logic functions on the chip is high. So VLSI chips are implemented using CMOS technology. Power dissipation will be the major problem in any of the circuits majorly in CMOS circuits it plays major role in the efficiency of the chip. The main reason to check amount of power dissipated because it effects the Performance, cost, packaging Reliability, portability of the chip. Power dissipation invariably leads to temperature rise of the chip. Temperature affects the device when it is in off state as well as when it is in on state. Where as in off state, number of intrinsic carriers in the region increases, by the following relation $n_i \propto \frac{e^{-EG}}{KT}$. Above relation shows that as temperature increases, it leads to increase in the number of intrinsic carriers in the semiconductor. Due rise in temperature majority carriers are less effected so the device becomes more intrinsic.

As temperature increases, leakage current which is directly dependent on minority carrier concentration increases which leads to further rise in temperature. This may cause device break down, if time to time removal of heat is not taken care by increase in temperature The main components of power dissipation are Static dynamic power dissipation, power dissipation, short circuit power dissipation**.** Reducing the clock frequency is not as easy task to perform and it is not as fruitful like reducing the supply voltage. Now a days, many advanced processors posse variant power-down modes where the clock signal is stationary to block the application that are idle at that instant. Above process is also known as clock gating which can be used in most cases as concurrence with other low-power techniques. Scaling the supply voltage is an

striking solution to deprive the power dissipation where both the switched and the short-circuit power dissipation have a strong dependency on threshold voltage.

A delay signal can be mitigated by reducing the threshold voltage but at that instinct the sub threshold leakage will increase exponentially.

Dynamic power dissipation is stated as the continuous charge and discharge of the load capacitance which leads to switching power dissipation. When the components of the system are at static state the circuits all start liberating the static power. The main components of static power dissipation mainly divide into sub-threshold current and reversed- biased diode leakage currents. When we operate on the down scaling of threshold voltage, the sub threshold leakage become prominent. Below the threshold voltage, in weak inversion state, the transistors are not completely off. The sub threshold current has a strong dependence on the threshold voltage.

Carry Look Ahead Adder

A Carry Look Ahead Adder is digital logic circuit which performs addition of binary bits. In carry look ahead adder time required to calculate the carry bits is reduced, so that speed of is increased. When CLA is compared with another adder which are usually slower. Carry bit and sum bit are calculated parallel. [5] When cascaded every bit must wait till the previous block carry is generated. For its own carry and results. In carry look ahead adder before sum all the carry bits are calculated, ultimately which results in the reduction of the lag time to evaluation the results in large value bits. In carry look ahead adder for calculation of carry two signals are used Generator and propagation. [5] Suppose A and B are inputs

$$G = A \cdot B$$

$$P = A \oplus B$$

Carry is denoted by C: $C_{i+1} = G_i + (\ P_i \cdot C_i)$

Following block diagram represents the basic blocks of carry look ahead adder.

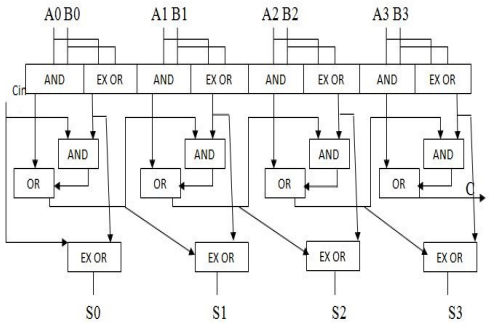


Figure 1: Basic Blocks of Carry Look Ahead Adder

Pseudo NMOS Logic

The CMOS pull up network is replaced by a single pMOS transistor with its gate grounded Since the pMOS is not driven by signals, it is always 'on'. [5] The effective gate voltage seen by the pMOS transistor is V_{dd} . Thus the overvoltage on the p channel gate is always V_{dd} - V_{Tp}. As we sweep the input voltage from ground to V_{dd} , we encounter the following regimes of operation nMOS 'off' nMOS saturated, pMOS linear nMOS linear, pMOS linear nMOS linear, pMOS saturated When the nMOS is turned 'on', a direct path between supply and ground exists and static power will be drawn. [7] However, the dynamic power is reduced When the input voltage is less than V_{Tn}. The output is 'high' and no current isdrawn from the supply. As we raise the input just above V_{Tn}, the output starts falling. In this region the nMOS is saturated, while the pMOS is linear [7].

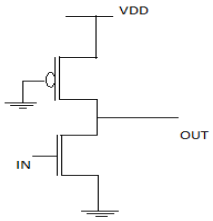


Figure 2: Pseudo NMOS logic Inverter

Domino logic style

At present environment, usage of dynamic circuit becomes popular. In Dynamic CMOS circuit in addition to the combinational logic inputs of static system will have clocked signal. When compared with static systems, dynamic systems are fast and efficient. [1][3] so domino logic is used in design of microprocessor. [1] But it has problem logic upset encountered due to charge loss of capacitor, this is not acceptable. Charge loss may also occur due to charge sharing, [4] charge leakage. When charge loss occurs it cannot be restored, this results in improper functioning. In dynamic circuit due to parasitic capacitance present at various nodes will results in charge sharing. This will cause lower voltage at output.[1][3] To realize a Boolean function we need several blocks of dynamic circuit. Same clock is applied for all the blocks of dynamic circuit due to resistance and parasitic capacitance present in the wire which carry clock causes delay this delay is different at different points of the circuit as delay is proportional to length of wire. [3] The operation of dynamic circuit can be divide in to two modes. [1] [3] They are precharge mode and evaluation mode In precharge mode (clock=0)output of the circuit is raised to logic high.[1][3][6] Evaluation mode(clock=1) occur when clock is high in evaluation mode there are two possibility. Discharge at the output node to logic low through NMOS, or remain high.[1][3][4] [6]dynamic gates are not used for cascading directly as output is precharged which cause output discharge fanout in next stage. [2] To eradicate this problem in cascading blocks a static inverter is used at the output of each block which will produce only non inverting blocks [2].

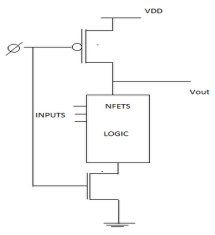


Figure 3: Basic structure of Dynamic Logic

Implementation of carry looks ahead adder using various logic styles

Conventional carry look ahead adder is designed using basic gates which are designed using complementary CMOS logic schematic diagram of it can be observed in Figure 4(a) it has eight inputs in which first four bits are added with second four bits which gives an output of four bits with carry. And in Figure 4(b) we can observe the layout of conventional carry look ahead adder following all the lambda rules.

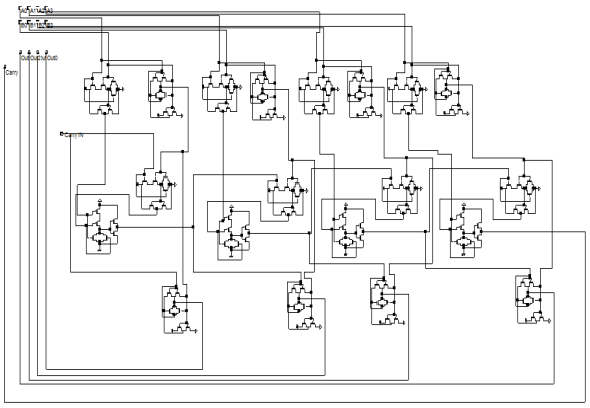


Figure 4(a): Schematic diagram of conventional carry look ahead adder

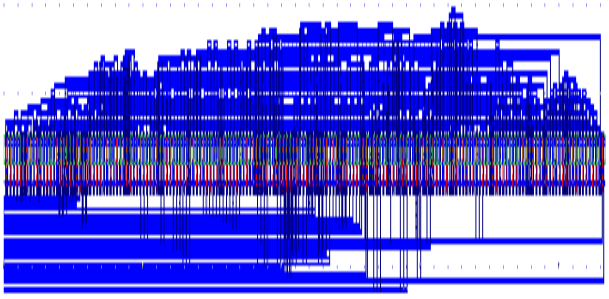


Figure 4(b): Layout of conventional Carry Look Head Adder

In Figure 5(a) schematic diagram of carry look ahead adder is represented it is designed using Pseudo nMos logic style. pull up network present in the complementary CMOS logic style is replaced with a single pMos connected to ground this pMos is always ON depending on the logic output will charge or discharge it will

reduce the area, where as it will dissipate power due to static power dissipation due to the bridge which comes into existence when both pull up and pull down networks are in ON condition. Figure 5(b) is layout of carry look ahead adder designed using Pseudo nMos logic style following all lambda rules.

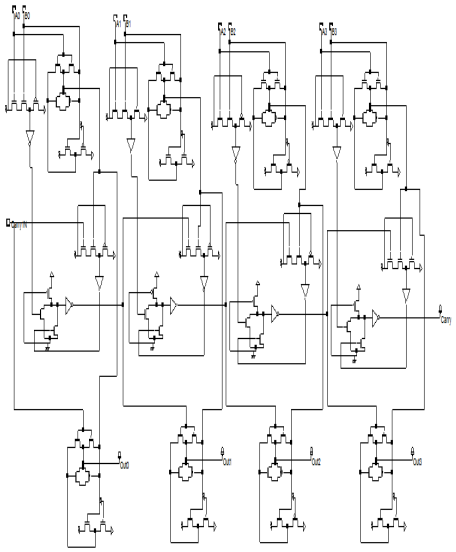


Figure 5(a): Schematic diagram of carry look ahead adder using Pseudo NMOS Logic

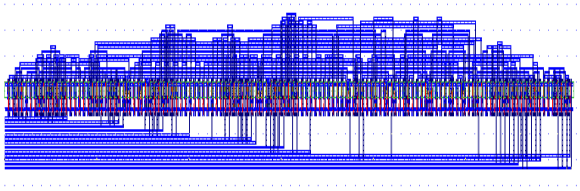


Figure 5(b): Layout of Pseudo NMOS logic Carry look ahead adder

Domino logic style is used to design carry look ahead adder this schematic diagram is represented in Figure 6(a) when we observe the schematic common clock is given to pull up pMos and pull down nMos while evaluating the logic block direct path between Vdd and GND is not possible as when pMos is ON nMos will be off vise versa takes place. Domino logic style eradicates the static power dissipation. Figure 6(b) is layout representation of domino logic carry look ahead adder following all lambda rules.

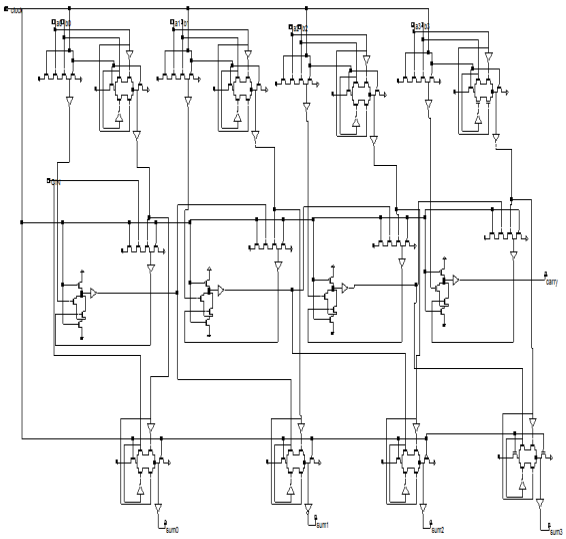


Figure 6(a): Schematic diagram of carry look ahead adder using domino logic

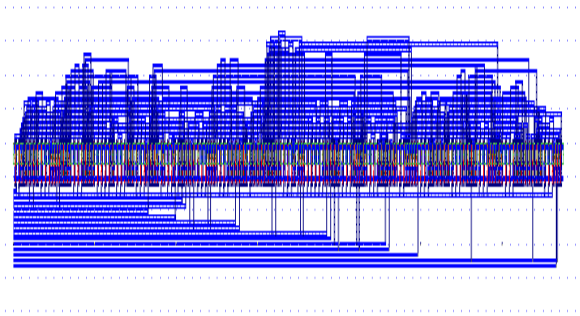
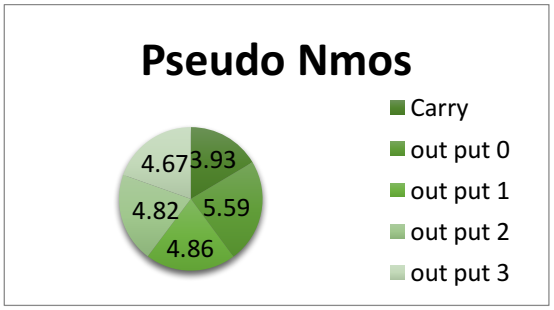
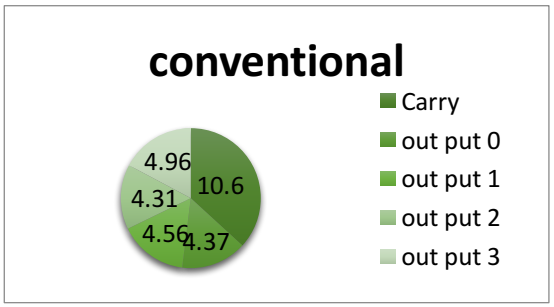
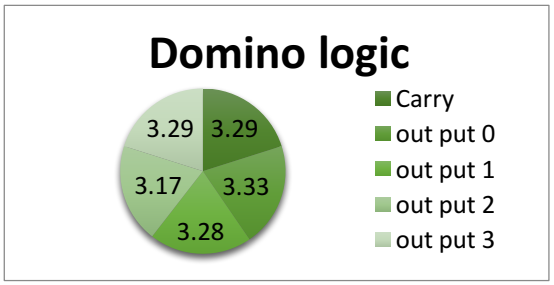


Figure 6(b): Layout of domino logic carry look ahead adder

Power Consumption of Carry look ahead adder in various Low power logic styles.







Conclusion

As per the observations conducted through our result analysis for the applications of low power CMOS logic styles such as pseudo NMOS, SR logic, domino, modified domino logic styles to the proposed CLA architecture. We interpret that modified domino logic style is efficient on to be applied to the CLA such that the power consumed is very low compared to the other CMOS logic styles to CLA. Apart from that we have observed the area has got reduced by applying Pseudo NMOS logic to CLA compared in area among all logic styles. When area is the main objective of the designer, Pseudo NMOS logic is efficient.

Table 1: Area Utilization and power comparison

Logic Styles		Transistors Required	Power Dissipation	
			Voltage	mW
CLA	Carry	120	4.8	10.67
	Out0			4.37
	Out1			4.56
	Out2			4.31
	Out3			4.96
Pseudo CLA	Carry	108	4.8	3.93
	Out0			5.59
	Out1			4.86
	Out2			4.82
	Out3			4.67
Domino logic	Carry	168	4.8	3.29
	Out0			3.33
	Out1			3.28
	Out2			3.17
	Out3			3.29

References

[1]. Themistoklis Haniotakis, Yiorgos Tsiatouhas, Dimitris Nikolos, and Constantine Efstathiou ||Testable Designs of Multiple Precharged Domino Circuits || IEEE transactions on very large scale integration (vlsi) systems, vol. 15, no. 4, april 2007

[2]. Chulwoo Kim, Seong-Ook Jung, Kwang-Hyun Baek, and Sung-Mo Kang || High-speed cmos circuits with parallel dynamic logic and speed-enhanced skewed static logic|| IEEE transactions on circuits and systems—ii: analog and digital signal processing, vol. 49, no. 6, june 2002

[3]. Vijaya bhaskar m, suparshya babu sukhavasi, susrutha babu sukhavasi, g santhi swaroop vemana . || Implementation of synchronous up counter by using self resetting logic || IJEAR Vol. 2, Issue 1,Jan-Feb 2012, pp.972-981

[4]. Shih-Chieh Chang, Member, IEEE, Ching-Hwa Cheng, Wen-Ben Jone, Member, IEEE, Shin-De Lee, and Jinn-Shyan Wang, Member, IEEE || Charge-sharing alleviation and detection for cmos domino circuits || IEEE transactions on computer-aided design

of integrated circuits and systems, vol. 20, no. 2, february 2001

[5]. Jagannath Samanta, Mousam Halder, Bishnu Prasad De ||Performance analysis of high speed low power carry look-ahead adder using different logic styles || IJSCE Volume-2, Issue-6, Jan- 2013

[6]. Ms. Rakhi R. Agrawal, Dr. S.A.Ladhake || Systematic Design of High-Speed and Low-Power Domino Logic || IJACSSE Volume 2, Issue 3, March 2012

[7]. Sandeep Sangwan, Mrs. Jyoti Kedia, Deepak Kedia || A comparative analysis of different cmos logic design techniques for low power and high speed || IJAREEIE Vol. 2, Issue 10, October 2013

[8]. Neil H.E. Weste, David Harris and Ayan Banerjee, "*CMOS VLSI Design,* A circuits and system perspective", (3rd Edition, Pearson Education,2005).

[9]. Kaushik Roy, Sharat C. Prasad , " Low-Power CMOS VLSI Circuit Design", John Wiley & Sons, 2009.